

MEMORY CHANNEL TEST FIXTURE AND METHOD

ABSTRACT OF THE DISCLOSURE

5 Method and apparatus for use with buffered memory modules are included among the embodiments. In exemplary systems, the memory module has a host-side memory channel port and a downstream memory channel port, allowing multiple modules to be chained point-to-point. In the present disclosure, a separate bus, such as a low-speed system management bus, connects to a memory module buffer. In response to commands received over the
10 system management bus, the memory module can initiate commands and transmit those commands over its downstream memory channel port as if the commands originated from a host connected to the host-side memory channel port. This functionality allows module-to-module memory channels and memory modules to be tested independent of a host memory controller and host memory channel. Other embodiments are described and claimed.